Amendments to the Specification:

Please amend the paragraph beginning on page 3 at line 18 as follows:

A1

Fig. 1B shows the example of the branch metric values M_1, M_2, M_3 and M_4 as 0.25, 0.1, 0.3 and 0.15, respectively, and the initial weights of old S_0 and old S_1 as 0.3 and ~~0.5~~ 0.4, respectively. The weights of new S_0 and new ~~S_4~~ S_8 after one step of encoding are 0.55 and 0.7, respectively, according to the following calculations:

$W(\text{new } S_0) = \max \{ 0.3 + 0.25, 0.4 + 0.1\} = 0.55$

$W(\text{new } S_4\ S_8) = \max \{ 0.3 + 0.15, 0.4 + 0.3\} = 0.7$

Please amend the paragraph beginning on page 24 at line 11 as follows:

A2

As is known in the art, steps 1302 and 1304 can be combined in a single cycle. Therefore, for the case of trace bits of a 16-state binary convolution decoder (i.e. a constraint length K of 5) saved sequentially in memory cells of length at least 16 bits, the trace back can be performed in as few as two cycles. This is as opposed to the six cycles required by the prior art method. The second cycle is step 1306. This achievement of as few as two cycles is due to the sequential arrangement of the trace bits in registers VTR0 and VTR1 and subsequently in the memory cells, and due to the new instruction that combines steps 1302 and 1304. In fact, any time the group of memory cells which stores the trace bits for all states of a stage is ~~a group of a~~ one memory cell, the trace back can be performed in as few as two cycles.

Please amend the paragraph beginning on page 24 at line 22 as follows:

A3

It will be appreciated by persons skilled in the art that register Y may be a shift ~~registers~~ register, in which case flag F is stored directly to the least significant bit of register Y. Alternatively, register Y may be a simple output register, in which case a barrel shifter is placed as an intermediary between flag F and register Y.